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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/001,472	11/01/2001	Robert H. Havemann	TI-27506	1913

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[REDACTED] EXAMINER

WOJCIECHOWICZ, EDWARD JOSEPH

ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 07/17/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 10/001,472	Applicant(s) Havermann
	Examiner Edward Wojciechowicz	Art Unit 2815

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) Responsive to communication(s) filed on _____.
- 2a) This action is FINAL. 2b) This action is non-final.
- 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

Disposition of Claims

- 4) Claim(s) 1-20 is/are pending in the application.
- 4a) Of the above, claim(s) 11-20 is/are withdrawn from consideration.
- 5) Claim(s) _____ is/are allowed.
- 6) Claim(s) 1-10 is/are rejected.
- 7) Claim(s) _____ is/are objected to.
- 8) Claims _____ are subject to restriction and/or election requirement.

Application Papers

- 9) The specification is objected to by the Examiner.
- 10) The drawing(s) filed on _____ is/are objected to by the Examiner.
- 11) The proposed drawing correction filed on _____ is: a) approved b) disapproved.
- 12) The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

- 13) Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

a) All b) Some* c) None of:

1. Certified copies of the priority documents have been received.
2. Certified copies of the priority documents have been received in Application No. _____.
3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

*See the attached detailed Office action for a list of the certified copies not received.

- 14) Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

Attachment(s)

- 15) Notice of References Cited (PTO-892) 18) Interview Summary (PTO-413) Paper No(s). _____
- 16) Notice of Draftsperson's Patent Drawing Review (PTO-948) 19) Notice of Informal Patent Application (PTO-152)
- 17) Information Disclosure Statement(s) (PTO-1449) Paper No(s). 2 20) Other: _____

Art Unit: 2815

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371© of this title before the invention thereof by the applicant for patent.

2. Claims 1-3, and 5 are rejected under 35 U.S.C. 102(e) as being anticipated by Oda.

Oda teaches the basic structure, and inventive concept of the invention with the formation of a porous dielectric material used in semiconductor devices, so as to reduce unwanted capacitance between conductors. See, for example, Fig. 5 of Oda where porous dielectric material (10) is formed between the semiconductor substrate and upper conductor layers, as claimed.

In addition, this oxide layer of Oda is doped with fluorine to render it porous, and Oda also shows a nitride layer (6) which is formed between the semiconductor device and the porous dielectric layer, as claimed.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

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(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. Claims 4 and 6-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Oda in view of Tseng. Although Oda does not identify particular types of semiconductor devices used in his structure, these would most likely include such common devices as field effect transistors, etc. However, in order to support this contention, Tseng is cited to specifically show such device structure as FETs with source/drain, and gate regions, etc. Furthermore, Tseng also teaches the use of porous oxides used with these devices, as referenced at col. 6, l. 46.

The motivation to combine these references comes from the basic recognition in Oda that such porous dielectric layers can improve all common types of semiconductor devices by reducing unwanted capacitance by lowering the dielectric constant of the dielectric materials used.

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to E. Wojciechowicz whose telephone number is (703) 308-4898, or to SPE Eddie Lee whose number is 703-308-1690.

EW:ew

July 15, 2002


EDWARD WOJCIECHOWICZ
PRIMARY EXAMINER